Title: Relaxed SiGe Platform for High Speed CMOS
Electronics and High Speed Analog Circuits
Inventor: Fitzgerald
Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
Formal Drawing Sheet 1 of 17

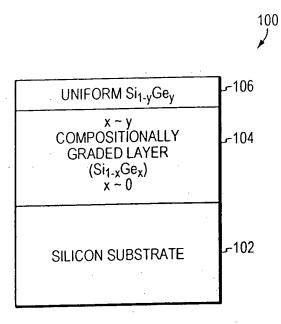


FIG. 1

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 2 of 17

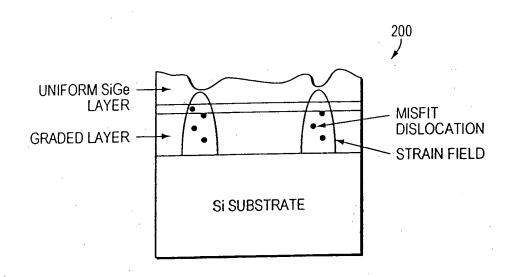


FIG. 2

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 3 of 17

3/17

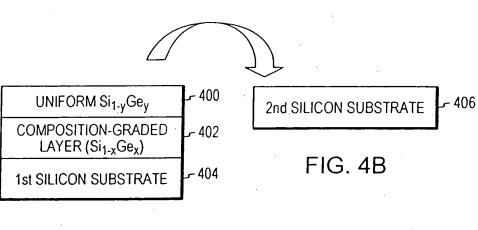
TYPE OF SURFACE	AVERAGE ROUGHNESS (nm)
AS-GROWN GRADED COMPOSITION RELAXED SiGe PLANARIZED SiGe REGROWTH SiGe, LATTICE-MATCHED REGROWTH SiGe, LIGHT MISMATCH, THICKNESS = 1.5 µm	7.9 0.57 ~0.6 0.77

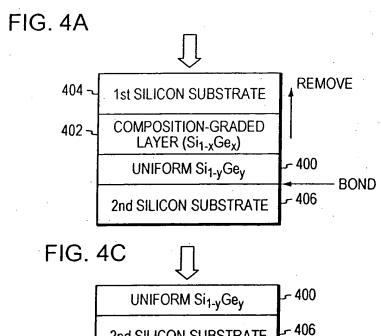
FIG. 3

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov

Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 4 of 17

4/17





2nd SILICON SUBSTRATE

FIG. 4D

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 5 of 17

5/17

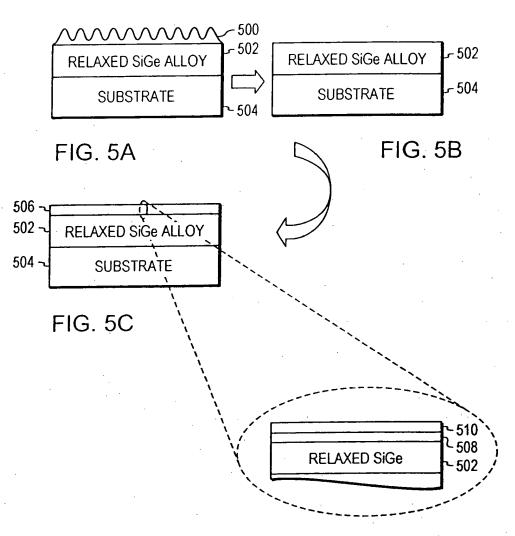
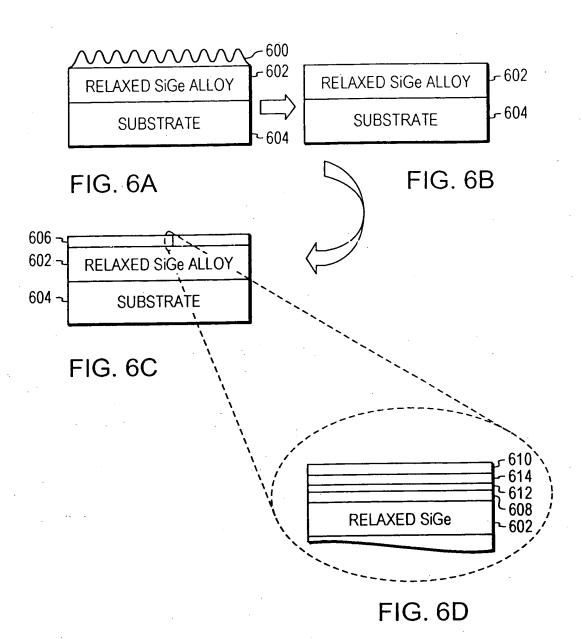


FIG. 5D

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald
Serial No.: Not Yet Assigned
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Express Mail Mailing Label No.: EL 988705761 US
Formal Drawing Sheet 6 of 17



Title: Relaxed SiGe Platform for High Speed CMOS
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Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
Formal Drawing Sheet 7 of 17

7/17

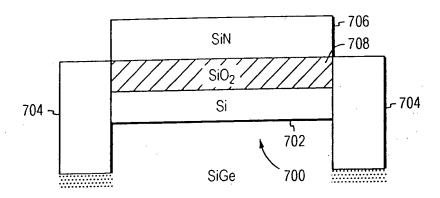


FIG. 7A

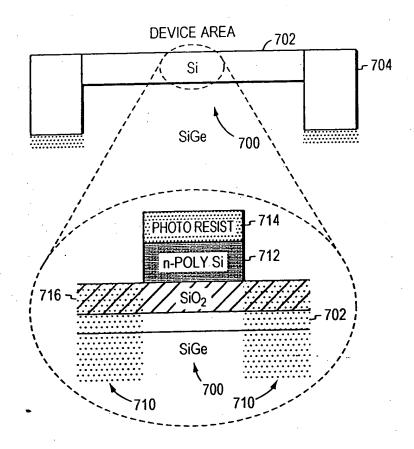


FIG. 7B

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald
Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
Formal Drawing Sheet 8 of 17

8/17

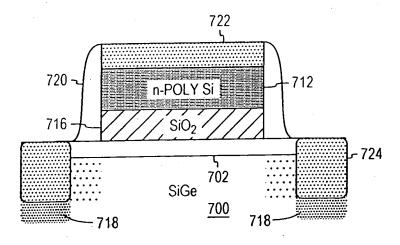


FIG. 7C

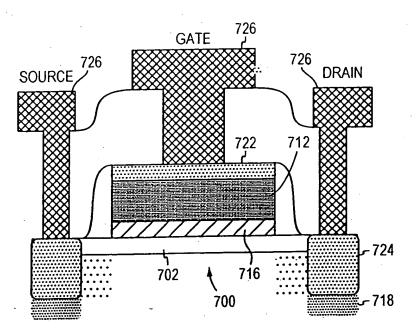


FIG. 7D

Title: Relaxed SiGe Platform for High Speed CMOS
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Formal Drawing Sheet 9 of 17

9/17

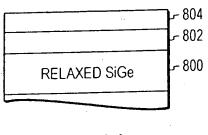


FIG. 8A



FIG. 8B

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 10 of 17

10/17

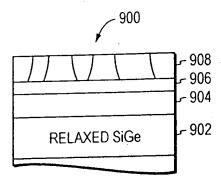


FIG. 9A

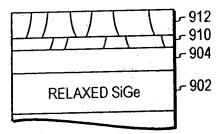


FIG. 9B

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 11 of 17

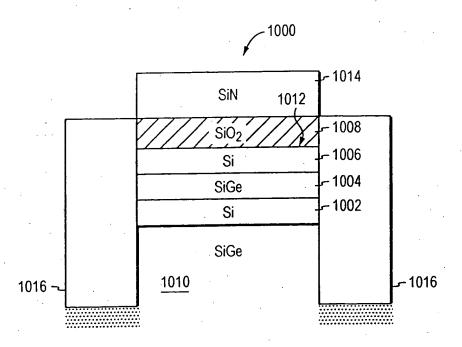


FIG. 10

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits

Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov

Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 12 of 17

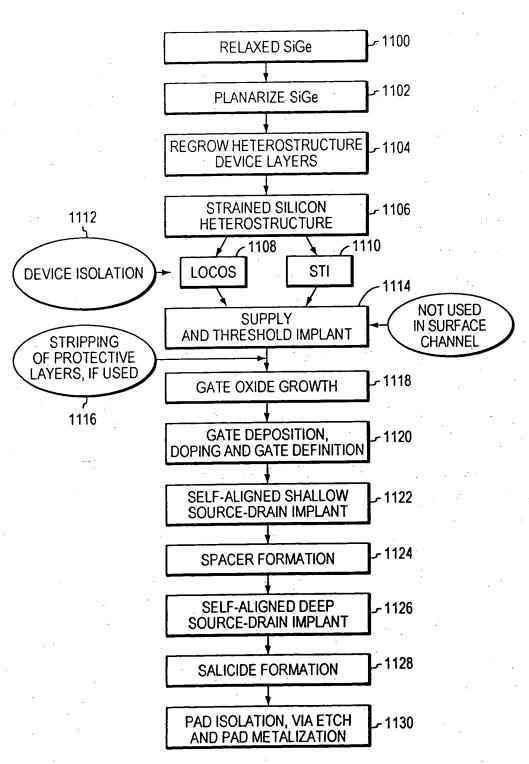


FIG. 11

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits

Inventor: Fitzgerald

Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1

Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 13 of 17

13/17

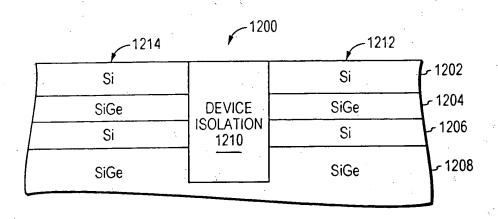


FIG. 12A

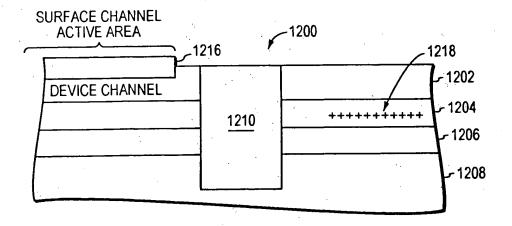


FIG. 12B

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald

Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov

Express Mail Mailing Label No.: EL 988705761 US
Formal Drawing Sheet 14 of 17

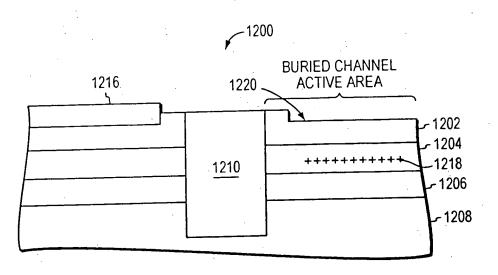


FIG. 12C

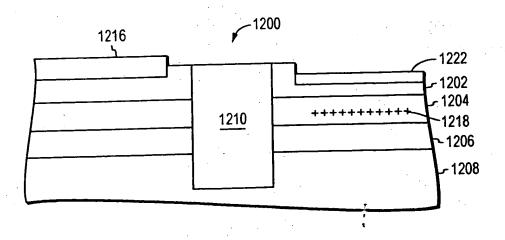


FIG. 12D

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov

Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 15 of 17

15/17

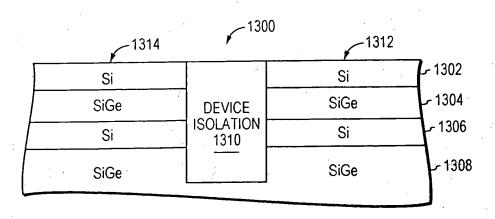
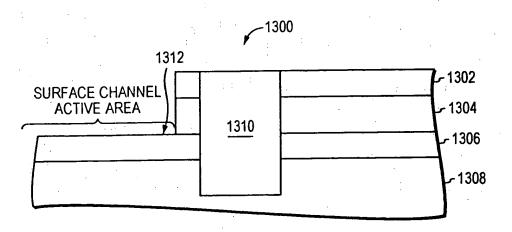


FIG. 13A



FIG; 13B

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald
Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
Formal Drawing Sheet 16 of 17

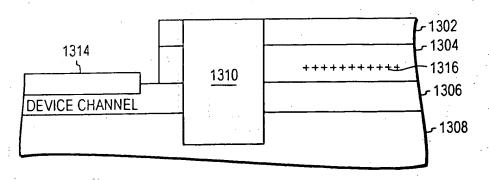


FIG. 13C

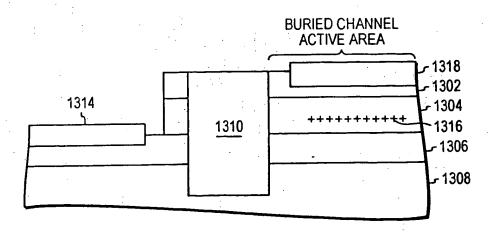


FIG. 13D

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 17 of 17

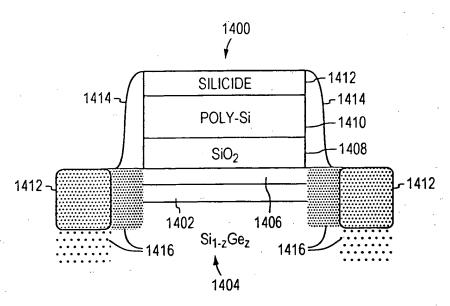


FIG. 14A

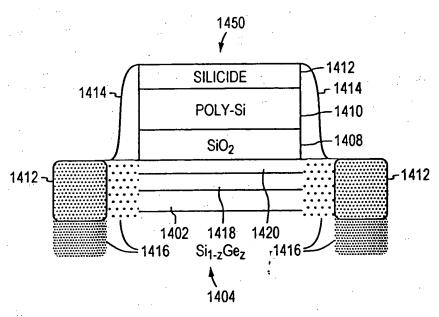


FIG. 14B